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10/803,174	03/16/2004	Bernd Barchmann	E0196.0005	4131

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EXAMINER	
NGUYEN, HOA CAO	
ART UNIT	PAPER NUMBER
2841	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/29/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/803,174	BARCHMANN ET AL.	
	Examiner	Art Unit	
	Hoa C. Nguyen	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-10,12,13,19-24 and 30-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-10, 12-13; 19-24, and 30-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 October 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 10/20/06 has been entered. Applicants have amended the drawings and claims 1 and 5. Claims 2, 11, 14-18, and 25-29 are cancelled.

Claims 1, 3-10, 12-13, 19-24, and 30-33 are treated on the merits in this Office action.

Drawings

2. The drawings (figures 9 and 10, page 8/8) were received on 10/20/06. These drawings are not accepted, because the "spacer 60" can not be found in the submitted drawings (see applicants' Remarks, page 8, 2nd paragraph). Furthermore, reference 60 is not disclosed in the specification to designated as a spacer.

The requirement is still deemed proper and is therefore made **FINAL**.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 5, the limitation "the contact areas of the contact-side metallization are shaped as defined in the International Organization for Standardization 7816-2 standard" is considered as indefinite, because a standard can be changed/modified from time to time. Furthermore, the term "International Organization for Standardization 7816-2 standard" is considered as a Trademark ("ISO"), therefore

the term should be replaced with a generic term that must clearly disclose the structure of the shape of the contact areas. It is also noted that the International Organization for Standardization 7816-2 standard is a standard that mainly discloses the standards of the electrical characteristic, the electrical level, and the role of each contact on a smart card.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 3-10, 12-13, 19-24, and 30-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huber et al. (US 6384425) in view of Kawan (US 6235553).

Regarding claim 1, as shown in figures 1-2, Huber discloses a nonconducting substrate 2 (col.3:36) forming a strip 1 (col.3:33) on which a plurality of carrier elements having respective boundary lines 4 (contour lines, col.3:51) are formed, comprising:

(a) A contact side (as shown in figure 1);

(b) an insertion side (as shown in figure 2);

(c) a conducting insertion-side metallization 9/10/11/14/15 (col.3:62; considering the listed conductors as conducting metallization) provided on the insertion side;

(d) a plurality of contact elements 10/11 (col.4:2 and col.4:15) provided on the insertion-side metallization within each boundary line 4,

(e) the contact elements are in a form of interconnects (as clearly shown in figure 2, connection between via holes or cutouts), which respectively have a first and a second end (arbitrarily selecting the left and the right end of each contact element as a first and a second end, for eaxmple), and at least some of the interconnects are provided with area-covering metallization (because the interconnects are formed of conductive metal material), which inherently serve for increasing the bending rigidity of the substrate.

But, Huber does not disclose the insertion-side metallization that is formed such that an electrical connection can take place by means of flip-chip bonding between contact points of an integrated circuit to be applied to the insertion side and the insertion-side metallization or the contact elements are at least partly for bonding with flip-chip contacts of the integrated circuit. Indeed, Huber discloses the insertion-side metallization is formed for wire-bonding instead.

However, flip-chip technology is old and well known in the art; therefore, it is only a matter of design choice depending upon particular applications to make the insertion-side for flip-chip bonding applications, and the contact points are easily used for flip-chip connections instead of wire-bonding connections. In such flip-chip applications, the contact points can be formed for having contact pads arranged to match with the array of the contacts of a flip-chip.

Kawan, as shown in figures 7-10, discloses a flip-chip technology for inserting a semiconductor chip on an insertion side of a smart card comprising a contact side and an insertion side (front side/rear side, figures 2-3, col.3:49-60), a conducting insertion-

side metallization 52-59 (bonding points, col.6:55) provided on the insertion side. Wherein the insertion-side metallization 52-59 is formed such that an electrical connection can take place by means of flip-chip bonding between contact points of an integrated circuit to be applied to the insertion side and the insertion-side metallization (col.6:48-col.8:65). It is noted that Kawan discloses multiple embodiments for both wire-bonding and flip-chip bonding (see figures 5-6 and 7-8).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the teachings about the flip-chip bonding from Kawan on the carrier elements of Huber in which the insertion-side metallization is formed such that an electrical connection can take place by means of flip-chip bonding between contact points of an integrated circuit to be applied to the insertion side and the insertion-side metallization and the contact elements are at least partly for bonding with flip-chip contacts of the integrated circuit in order extend the capability of the carrier elements for flip-chip technology which is widely in use in the industry, and to also save cost in assembling because the steps for wire-bonding connections can be skipped.

Regarding claim 3, as shown in figure 1, Huber further discloses a contact-side metallization 8 (metal lines, col.3:56) provided on of the contact side of the substrate.

Regarding claim 4, as shown in figure 1, Huber further discloses a plurality of contact areas 5 (contact surfaces, col.3:53-54), which are electrically isolated from one another and are provided on the contact-side metallization within each boundary line 4 (outer contour line, col.3:52).

Regarding claim 5, the limitation "the contact areas of the contact-side metallization are shaped as defined in the International Organization for Standardization 7816-2 standard" is a standard that regards to the electrical characteristic of a smart card and to specify the electrical level and the role of each contact on the smart card. Because the discussed standard is merely an application or at least an intended of use of the contact elements, therefore the limitation is interpreted to only require the ability to so perform. In the case of product claim, only the structure of the claim distinguishes over the prior art. Thus, the claim is not patentable over Huber in view of Kawan.

Regarding claim 6, as shown in figure 2, Huber further discloses a plurality of contact elements 10/11 (col.4:2 and col.4:15) provided on the insertion-side metallization within each boundary line 4, wherein the contact areas of the contact-side metallization have at least partly an electrical connection with the contact elements of the insertion-side metallization (in order to test the semiconductor chip, see cut outs 12-13, col.3:64-col.4:15).

It is noted that the limitation "at least partly for bonding flip-chip contacts of the integrated circuit" is interpreted to only require the ability to so perform. In the case of product claim, only the structure of the claim distinguishes over the prior art.

Regarding claim 7, as shown in figure 2, Huber further discloses the electrical connection, which is established by plated-through holes 12-13 (col.3:64-col.4:15 and col.5:13) extending through the substrate.

Regarding claim 8, as shown in figures 1-2, Huber discloses the plated-through holes that are each arranged in a plated-through region (arbitrary selected areas within the metal contact areas 5) of the contact areas of the contact-side metallization that is inherently not intended for bonding with an external reader.

Regarding claim 9, as shown in figures 1-2, Huber further discloses a boundary line region 4, which includes the contact-side metallization 5 and inherently brings about an increased moment of resistance in a region of the integrated circuit.

Regarding claim 10, as shown in figures 1-2, Huber discloses the boundary line region crosses a line of symmetry (considering a line dividing the area within the boundary 4 in haft), which is formed between oppositely lying contact areas of the contact-side metallization.

Regarding claim 12, as shown in figure 2, Huber discloses the contact elements of the insertion-side metallization that are in a form of interconnects (as shown in the figure), which respectively have a first end and a second end (all conducting elements have first and second ends, wherein first and second ends are arbitrary defined), the first end (arbitrarily selected contact area around the cut-out 13 as a first end) of the interconnects overlapping with a respective one of the plated-through holes 13 and being in electrical connection therewith.

Regarding claim 13, as shown in figure 2, Huber in view of Kawan, discloses the second end (arbitrarily selected contact area 11 as a second end) has a first contact area 11 for the electrical bonding with a flip-chip contact of the integrated circuit.

Regarding claim 19, as shown in figure 2, Huber discloses the area-covering metallizations are formed within the boundary line 4 of the respective carrier element.

Regarding claim 20, as shown in figure 2, Huber discloses the area-covering metallizations are provided in a region outside the integrated circuit to be applied.

Regarding claim 21, as shown in figure 1, Huber discloses indexing holes 3 (perforations, col.3:41), which are provided on the substrate, and inherently to stiffen the substrate, are surrounded by metallizations 8 (col.3:55) on the insertion side and/or the contact side.

Regarding claim 22, as shown in figure 2, Huber discloses adjusting marks (no number, considering the bar connecting index holes 3 as an adjusting mask), which constitute part of the insertion-side metallization and are provided on the substrate for orientation of placement machines.

Regarding claim 23, as shown in figure 2, Huber further discloses transverse webs 8 (considering line 8 which runs in between left and right carrier elements) which constitute part of the insertion-side metallization and are provided on the substrate between neighboring carrier elements.

Regarding claim 24, Huber in view of Kawan discloses in a region of the integrated circuit to be applied, the insertion-side metallization inherently comprises spacers (formed by solder balls that electrically connecting a semiconductor chip and the insertion side metallization), which inherently ensure plane-parallelism between the integrated circuit and the insertion side of the substrate.

Regarding claim 30, Huber discloses the substrate 2 (col.3:36) consisting of glass fiber-reinforced epoxy resin (a thermoplastic resin), which is PEN.

Regarding claim 31, Huber discloses every limitation as shown in claim 30 above, but does not disclose the thickness of the substrate.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to select a thickness of the substrate to be within 50 to 125 .mu.m for a specific application, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding claim 32, the limitation "the contact-side metallization and the insertion-side metallization are produced by a growing-on process" is regarded as process claim limitation in a product claim and is treated in accordance with MPEP 2113. As this process limitation results in a product structure that is the same as the product of Nakamura et al., therefore Huber anticipates the claim.

Regarding claim 33, Huber does not disclose the thickness of the contact-side metallization and the insertion-side metallization.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to select a thickness of the contact-side metallization and the insertion-side metallization to be less than 40 mu.m for a specific application, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Response to Arguments

7. Applicant's arguments filed 10/20/06 have been fully considered but they are not persuasive.

Remarks, page 9, 2nd-3rd paragraph: The argument centers about the lines 15 that do not represent contact elements bonding with flip-chip contacts of the integrated circuit.

Huber does not disclose the insertion-side for flip-chip bonding but Kawan does. Kawan teaches that an insertion-side having wire-bonding configurations (figures 5-6) can be changed for flip-chip bonding (figures 7-10).

Regarding the line 15, the conductor line 15 represents connections between contact areas and it is merely for illustration purpose. Every circuit pattern has conductive lines for interconnections between contact points. Furthermore, line 15 is not a contact element; it is a conductive connecting element (see figure 2 again). And, the conductor material of the line 15 by itself (made of metal material) inherently serves for increasing the bending rigidity of the substrate.

Moreover, applicants have used non-selected structure disclosed in figure 6 in the arguments. It is to remind the applicants that figure 6 shows the structure of the insertion-side of the 2nd embodiment (figure 3 shows the contact side of the 2nd embodiment), and the details of the structure shown in figure 6 are not the same as the details of the structure shown in figure 9 (the insertion-side of the 3rd embodiment). Applicants are also noted that the structures disclosed in figures 7-9 were selected for

examination, see Office action mailed on 3/21/06 and applicants' Response to Election/Restriction filed on 5/12/06.

Examiner remarks: The claims fail to recite any structure limitation (especially claim 1) with the regard to the details of the contact-side and the insert-side that would keep the claims from reading on the interpretation of the reference that the contact elements (24 and 25 of figure 9, 3rd embodiment) read on the conductor structure 11 that has cutouts 12 formed therein (figure 2 of the reference). It is also noted that the vias 22 are formed space apart from the contact elements 24/25 and the vias 22 are formed outside the areas-covering metallization 27 (see figure 9).

Conclusion

8. Applicant's amendment necessitated the new ground(s) / new explanation of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoa C. Nguyen whose telephone number is 571-272-8293. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard, can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Hoa C. Nguyen
12/15/06

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